REMARKS

Claims 1-11, 13-18, 20-21, 23-49, 51-52, and 57-59 were previously pending in this patent application. Claims 1-11, 13-18, 20-21, 23-49, 51-52, and 57-59 stand rejected. Herein, no Claim has been amended. Accordingly, after this Amendment and Response, Claims 1-11, 13-18, 20-21, 23-49, 51-52, and 57-59 remain pending in this patent application. Further examination and reconsideration in view of the claims, remarks, and arguments set forth below is respectfully requested.

35 U.S.C. Section 103(a) Rejections

Claims 1-11, 13-18, 20-21, 23-49, 51-52, and 57 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Insenser Farre et al., U.S. Patent No. 6,460,172 (hereafter Insenser) in view of Furtek et al., U.S. Patent No. 5,894,565 (hereafter Furtek) and in view of van der Wal et al., U.S. Patent No. 6,188,381 (hereafter van der Wal) . These rejections are respectfully traversed.

Independent Claim 1 recites (as amended):

A microcontroller circuit comprising:
a bus;
a microprocessor coupled to said bus;
a memory coupled to said bus, wherein said memory comprises a non-volatile memory; and
a plurality of functionalities coupled to said bus, wherein said non-volatile memory functions to program said functionalities and wherein said plurality of functionalities comprise:
an interconnect wherein said interconnect is dynamically configurable and programmable;
an analog functional block coupled to said interconnect wherein said analog function block is dynamically configurable and programmable to perform one or more of a plurality of various analog functions; and
a dynamically configurable and programmable digital functional block coupled to said interconnect, wherein said

dynamically configurable and programmable digital functional block ***is configurable to perform any one of a plurality of predetermined digital functions upon being configured with a single register write operation***. (emphasis added)

It is respectfully asserted that the combination of Insenser, Furtek, and van der Wal does not teach, suggest, or motivate the present invention as recited in Independent Claim 1. In particular, the Independent Claim 1 recites the limitation, "said dynamically configurable and programmable ***digital functional block is configurable to perform any one of a plurality of predetermined digital functions upon being configured with a single register write operation***," (emphasis added). At page 5 of the Office Action, it is stated that neither Insenser nor Furtek specifically shows the single register write operation as claimed in Independent Claim 1. Further, it is argued at page 5 that van der Wal teaches a reconfigurable system including a single control register write for reconfiguring all functional blocks or devices, citing Col. 10, lines 30-38 of van der Wal. As will be explained below, van der Wal defines "reconfigurable" to have two separate meanings, where only one of the meanings includes configuration with control registers and where the other meaning includes configuration to perform different hardware functions. Therefore, the statement "a reconfigurable system including a single control register write for reconfiguring all functional blocks or devices" is inconsistent with and unsupported by van der Wal.

Continuing, van der Wal specifies that the term "reconfigurable" has been given two meanings, namely: type 1 "reconfigurable" devices having control registers which may be programmed to a new structure and type 2 "reconfigurable" devices such as FPGAs which are reconstituted to perform a different hardware function. [van der Wal; Col. 6, lines 36-41]. That is, type 2

"reconfigurable" devices perform different functions after being reconfigured while type 1 "reconfigurable" devices perform the same function (e.g., providing a data path between ports) with different structures (e.g., data path I between port A and port B, data path II between port A and port C, etc.) configurable by control registers. In the citation Col. 10, lines 30-38 of van der Wal, the "reconfigurable" device is configurable with one control register write. That is, the citation Col. 10, lines 30-38 of van der Wal refers to type 1 "reconfigurable" devices having control registers which may be programmed to a new structure instead of referring to type 2 "reconfigurable" devices such as FPGAs which are reconstituted to perform a different hardware function. Since Independent Claim 1 is directed to a digital functional block that is configurable to perform any one of a plurality of predetermined digital functions upon being configured with a single register write operation, it is clear that only type 2 "reconfigurable" devices of van der Wal are capable of being configured to perform different functions as the digital functional block of the invention of Independent Claim 1.

The fact that van der Wal specifies two types of "reconfigurable" devices (e.g., type 1 "reconfigurable" devices may be programmed to a new structure but same function, type 2 "reconfigurable" devices may be reconstituted to perform a different hardware function) and the fact that van der Wal only describes one type of "reconfigurable" devices (i.e., type 1 "reconfigurable" devices) as being configurable with one control register write, clearly indicate that type 2 "reconfigurable" devices are not configurable with a single register write operation and teache away from the type 2 "reconfigurable" devices being configurable with a single register write operation. Moreover, van der Wal states that type 2 "reconfigurable" devices such as FPGAs are reconfigurable for different hardware functions, where the reconfiguration is from software on one

or more of the processors (12) of the Processor Motherboard (10) through a JTAG interface. [van der Wal; Col. 13, lines 38-42; Col. 30, lines 35-37]. Thus, van der Wal does not teach, suggest, or motivate that a digital functional block is configurable to perform any one of a plurality of predetermined digital functions upon being configured with a single register write operation, as in the invention of Independent Claim 1.

As described above, the combination of Insenser, Furtek, and van der Wal does not teach, suggest, or motivate all the limitations of Independent Claim 1. Therefore, it is respectfully submitted that Independent Claim 1 is patentable over the combination of Insenser, Furtek, and van der Wal and is in condition for allowance.

Dependent Claims 2-10 are dependent on allowable Independent Claim 1, which is allowable over the combination of Insenser, Furtek, and van der Wal. Hence, it is respectfully submitted that Dependent Claims 2-10 are patentable over the combination of Insenser, Furtek, and van der Wal for the reasons discussed above.

With respect to Independent Claims 11, 17, 35, 37, 42, 51, and 52, it is respectfully submitted that Independent Claims 11, 17, 35, 37, 42, 51, and 52 recite similar limitations as in Independent Claim 1. In particular, Independent Claims 11, 17, 35, 37, 42, 51, and 52, are directed to digital logic whose digital function is "configured ***with a single register write operation***," (emphasis added). The combination of Insenser, Furtek, and van der Wal does not teach, suggest, or motivate all the limitations of Independent Claims 11, 17, 35, 37, 42,

51, and 52. Therefore, it is respectfully submitted that Independent Claims 11, 17, 35, 37, 42, 51, and 52 are patentable over the combination of Insenser, Furtek, and van der Wal and are in condition for allowance for reasons discussed in connection with Independent Claim 1.

Dependent Claims 13-16, 18, 20-21, 23-34, 36, 38-41, 43-49, and 57 are dependent on allowable Independent Claim 11, 17, 35, 37, 42, 51, and 52, which are allowable over the combination of Insenser, Furtek, and van der Wal. Hence, it is respectfully submitted that Dependent Claims 13-16, 18, 20-21, 23-34, 36, 38-41, 43-49, and 57 are patentable over the combination of Insenser, Furtek, and van der Wal for the reasons discussed above.

Claims 58-59 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Insenser Farre et al., U.S. Patent No. 6,460,172 (hereafter Insenser) in view of Gamal et al., U.S. Patent No. 5,754,826 (hereafter Gamal) and in view of van der Wal et al., U.S. Patent No. 6,188,381 (hereafter van der Wal). These rejections are respectfully traversed.

Independent Claim 58 recites (as amended):

> In a system disposed in an integrated circuit, said system comprising:
> a microcontroller comprising a non-volatile program memory;
> a subsystem coupled to said non-volatile program memory, comprising a plurality of analog functionalities and of digital functionalities that are both configurable according to a user input wherein said analog functionalities are programmable to perform one or more of a plurality of various analog functions and wherein said analog functionalities and said digital functionalities are programmed with code stored in said non-volatile program memory, wherein each digital functionality ***is configurable to perform any one of a plurality of predetermined digital***

functions upon being configured with a single register write operation;

an interconnecting mechanism configurable for selectively interconnecting said plurality of analog functionalities and said plurality of digital functionalities according to said user input; and

a coupling mechanism coupled to said subsystem that is configurable to implement a connectability state for said system by which said system is connectable to an external entity according to said user input, a method of configuring said system comprising:

a) selecting a function from the list consisting of analog functions, digital functions, and; mixed analog and digital functions

b) selecting an interconnection state to effectuate an interconnection between said analog functionalities and said digital functionalities corresponding to said function;

c) selecting said connectability state to effectuate an connection between said system and an external entity corresponding to said function; and

d) implementing said function, said interconnection state, and said connectability state according to said a), said b) and said c). (emphasis added)

It is respectfully asserted that the combination of Insenser, Gamal, and van der Wal does not teach, suggest, or motivate the present invention as recited in Independent Claim 58. In particular, the Independent Claim 58 recites the limitation, "each digital functionality ***is configurable to perform any one of a plurality of predetermined digital functions upon being configured with a single register write operation***," (emphasis added). At page 23 of the Office Action, it is stated that neither Insenser nor Gammal specifically shows the single register write operation as claimed in Independent Claim 58. Further, it is argued at pages 23-24 that van der Wal teaches a reconfigurable system including a single control register write for reconfiguring all functional blocks or devices, citing Col. 10, lines 30-38 of van der Wal. For the reasons explained above with respect to Independent Claim 1, van der Wal does not teach, suggest, or motivate that each digital functionality is configurable to perform any one of a plurality of predetermined digital functions upon being configured with a single register write operation, as in the invention of Independent Claim 58.

As described above, the combination of Insenser, Gamal, and van der Wal does not teach, suggest, or motivate all the limitations of Independent Claim 58. Therefore, it is respectfully submitted that Independent Claim 58 is patentable over the combination of Insenser, Gamal, and van der Wal and is in condition for allowance.

Dependent Claim 59 is dependent on allowable Independent Claim 58, which is allowable over the combination of Insenser, Gamal, and van der Wal. Hence, it is respectfully submitted that Dependent Claim 59 is patentable over the combination of Insenser, Gamal, and van der Wal for the reasons discussed above.

CONCLUSION

It is respectfully submitted that the above claims, arguments and remarks overcome all rejections and objections. All remaining claims (Claims 1-11, 13-18, 20-21, 23-49, 51-52, and 57-59) are neither anticipated nor obvious in view of the cited references. For at least the above-presented reasons, it is respectfully submitted that all remaining claims (Claims 1-11, 13-18, 20-21, 23-49, 51-52, and 57-59) are in condition for allowance.

The Examiner is urged to contact Applicant's undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Please charge any additional fees or apply any credits to our PTO deposit account number: 23-0085.

Respectfully submitted,

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Dated: 5/22/2006

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